MOTOROLA
Semiconductor Products Inc.

AN-889
Application Note

MC14500B DEVELOPMENT SYSTEM

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INTRODUCTION

An easy-to-use development system is a basic tool for the engineer utilizing a microprocessor in a system design. The scope of this application note is to describe such a system for the MC14500B (the Demonstration System Kit* is no longer available). This new development system has the following features: (1) keyboard data/address entry, (2) wide supply voltage range, (3) seven-segment readout, (4) 100% CMOS, and (5) accommodation of 256 program steps. The only disadvantage is that the new development system is not available in kit form; however, the designer can easily wirewrap the development system. The wirewrapped system offers increased flexibility for expansion and future modifications.

Recommended prerequisite reading is the "Industrial Control Unit Handbook".

SYSTEM BLOCK DIAGRAM

Figure 1 illustrates the development system in block diagram form. The program counter and memory may be conveniently loaded from the hex keypad. Both the program counter and the memory contents are displayed on hex displays for ease of interpretation. A selector is included for routing either simulated (switch) inputs or "real world" inputs to the system. The system outputs are displayed via LEDs and may be connected to controlled equipment.

The MC14500B has two software controllable outputs redefined for this development system. "NOPF" or "FLAG F" is redefined as "reset output latches." "Return" is redefined as "reset program counter." Note that execution of the "return" instruction causes the next instruction (at location hex 00) to be skipped. Therefore, the user's program must start at $01 (hex 01). In addition, $00 should be programmed as opcode 1, address F to insure that the result register LED is extinguished when in the battery back-up mode.

The power failure detector clears all registers internal to the MC14500B, holds the FLAG signals at a low level, stops the MC14500B oscillator, resets the program counter, and blanks the displays. Battery back-up prevents the contents of memory from being lost by providing quiescent current to the CMOS circuitry.

The instruction and address are displayed simultaneously on the seven-segment readouts. Either one or both may be changed while at a particular memory location.

SYSTEM LOGIC

Figures 2 and 3 illustrate the system logic diagrams. The only IC which is limited to operation from 3 to 6 volts is U1 (MC14419); therefore, with U1 removed (after the program is loaded), the system may be operated up to 15 volts as long as the seven-segment displays are not overdriven. Resistors R1 through R8 are provided to prevent damage to other components when U1 is removed. If a keypad with DPST normally open switches cannot be easily acquired, an SPST keyboard may be used in conjunction with four bipolar transistors, as shown in Figure 4.

Data is entered via the hex keypad, encoded by U1, and presented to the preload inputs of counters U4 and U5 and the memory data inputs of U21 through U28. A single load strobe (STROBE) is generated for each key depression by U18, U15, U2, and U17. STROBE is then steered by AND gates U20 to the memory or counters. Depressing the load select switch S1 controls the alternate steering of STROBE to program counter load strobe (PC-LOAD-STB) or memory load strobe (MEM-LOAD-STB). PC-LOAD-STB is then steered via AND gates U14 to the present enable inputs of program counters U4 and U5. Preset enables PE1 and PE2 are alternately generated for the counters as controlled by the keypad depression. Status LEDs D4 and D5 indicate whether the program counter or the memory is to be loaded from the keypad.

The outputs of the program counter are interfaced to seven-segment readouts via hexadecimal to seven-segment drivers U7 and U8. Q1 and Q2 insure that the readouts are

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*Described in the "Industrial Control Unit Handbook" (available from Motorola), reference Chapter 5 and Appendix B.

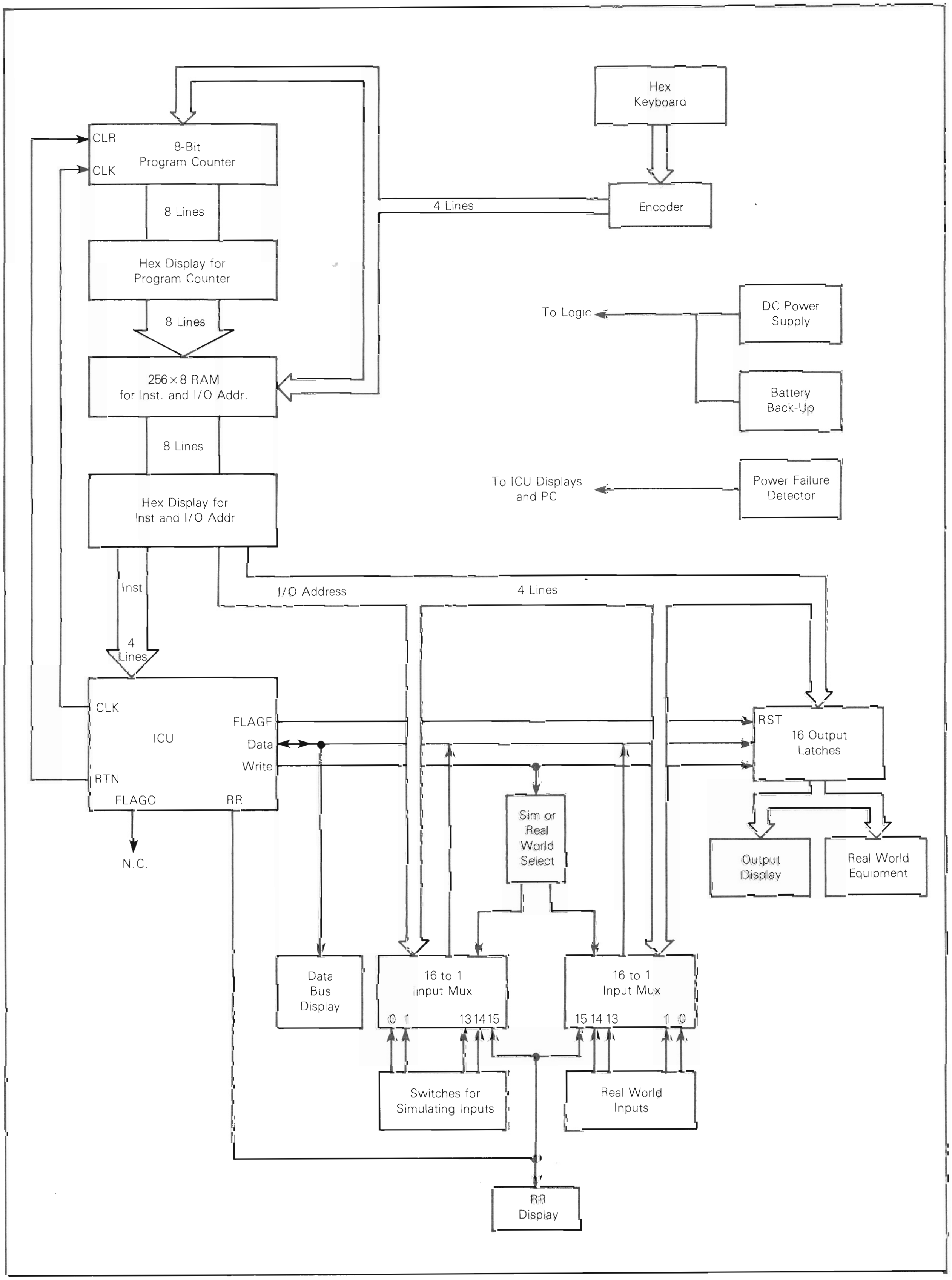

FIGURE 1. System Block Diagram

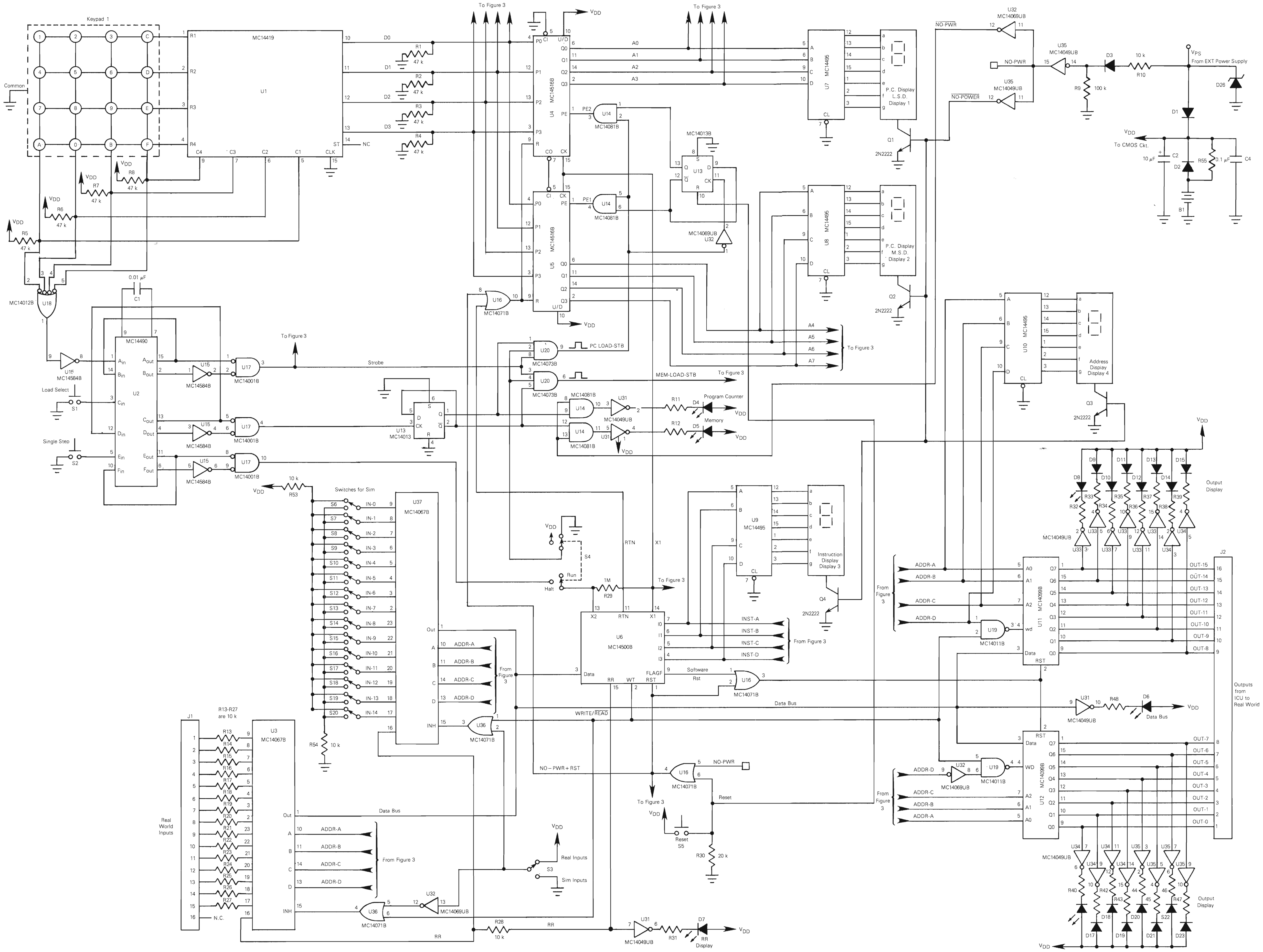

FIGURE 2. System Logic Diagram

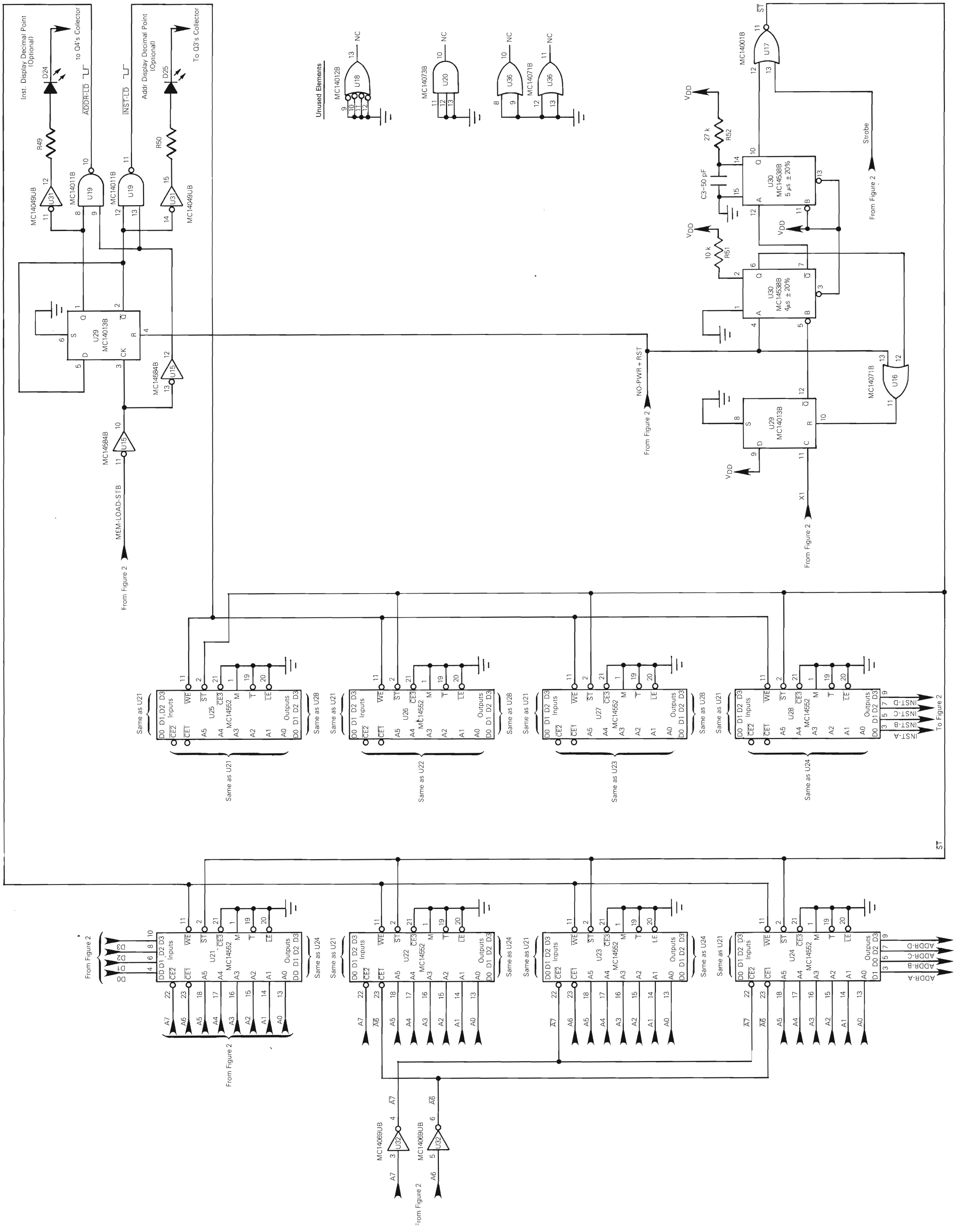

FIGURE 3. System Logic Diagram (Continued)

TABLE 2. Parts List

B1	Nicad Batteries, Number of Cells Depends on Supply Voltage Desired
C1	0.01 µF, 50 WVDC Ceramic Capacitor
C2	10 µF, 50 WVDC Electrolytic Capacitor
C3	50 pF, 50 WVDC Ceramic Capacitor
C4	0.1 µF, 50 WVDC Ceramic Capacitor
D1, D2, D3	1A Silicon Diode
D4 Through D23	LED
D24, D25	Decimal Points in Display 3 and 4
D26	Transient Suppressor Zener Diode, Depends on Supply Voltage (MPTE−5=5 V, MPTE−8=8 V, etc.)
Display 1 Through 4	Common Cathode Seven-Segment LED Display
J1, J2	16 Contact Socket
Keypad 1	Hex Keypad with DPST N.O. Switches
Q1, Q2, Q3, Q4	2N2222 Transistor
R1 Through R8	47 kΩ ±10%, ¼ Watt Resistor
R9	100 kΩ ±10%, ¼ Watt Resistor
R10	10 kΩ ±10%, ¼ Watt Resistor
R11, R12	Value Depends on Supply Voltage and D4, D5
R13 Through R28	10 kΩ ±10%, ¼ Watt Resistor
R29	1 MΩ ±10%, ¼ Watt Resistor
R30	20 kΩ ±10%, ¼ Watt Resistor
R31 Through R48	Value Depends on Supply Voltage and D7, D8 Through D23, D6
R49, R50	Value Depends on a Supply Voltage and Display 3, Display 4 Decimal Points
R51	10 kΩ ±10%, ¼ Watt Resistor
R52	27 kΩ ±10%, ¼ Watt Resistor
R53, R54	10 kΩ ±10%, ¼ Watt Resistor
R55	Value Depends on Charging Current Desired for B1
S1, S2	SPST N.O. Pushbutton Switch
S3	SPDT Toggle Switch
S4	DPDT Toggle Switch
S5	SPST N.O. Pushbutton Switch
S6 Through S20	SPDT Toggle Switch
U1	MC14419P
U2	MC14490P
U3	MC14067BCP
U4, U5	MC14516BCP
U6	MC14500BCP
U7, U8, U9, U10	MC14495P1
U11, U12	MC14099BCP
U13	MC14013BCP
U14	MC14081BCP
U15	MC14584BCP
U16	MC14071BCP
U17	MC14001BCP
U18	MC14012BCP
U19	MC14011BCP
U20	MC14073BCP
U21 Through U28	MCM14552CP
U29	MC14013BCP
U30	MC14538BCP
U31	MC14049UBCP
U32	MC14069UBCP
U33, U34, U35	MC14049UBCP
U36	MC14071BCP
U37	MC14067BCP
Misc.	DIP Sockets, Power Supply, Wire, Etc.

NOTE: Part numbers given for D26 and U1 Through U37 are Motorola numbers.

V_{SS}, OUT-O is extinguished. This program may also be used to check the real world inputs at connector J1, depending on the position of the "sim or real world select" switch (S3).

To load the program, switch the system to halt and hit reset. If the program counter LED is on, depress the load select switch; the memory LED will then turn on. Now, load location $00 with $1F (instruction/address) using the hex keypad. Check the displays for $1F in location $00. Next, depress the single step switch and load location $01 with $6F; repeat through location $22. After $22 is loaded with $DD, depressing the single step switch will cause the system to execute a reset program counter instruction ($DD) and the program counter display should indicate $00.

The programming entries can now be verified by single stepping through the program. Depressing the single step switch causes execution of the instruction displayed before depression and incrementation to the next memory location.

Now, switch the system to run. For S3 in the "sim inputs" position, switching the input simulation switches S6 through S20 should affect each of the corresponding output LEDs (0 through 14).

PC	Inst/Addr	Comment
$00	$1F	RR ← RR = 0 During Battery Backup Only (RR LED Off)
$01	$6F	RR ← RR + $\overline{RR}$ = 1
$02	$BF	Enable Outputs
$03	$AF	Enable Inputs
$04	$10	RR ← Input 0
$05	$80	RR → Output 0
$06	$11	RR ← Input 1
$07	$81	RR → Output 1
$08	$12	RR ← Input 2
$09	$82	RR → Output 2
$0A	$13	RR ← Input 3
$0B	$83	RR → Output 3
$0C	$14	RR ← Input 4
$0D	$84	RR → Output 4
$0E	$15	RR ← Input 5
$0F	$85	RR → Output 5
$10	$16	RR ← Input 6
$11	$86	RR → Output 6
$12	$17	RR ← Input 7
$13	$87	RR → Output 7
$14	$18	RR ← Input 8
$15	$88	RR → Output 8
$16	$19	RR ← Input 9
$17	$89	RR → Output 9
$18	$1A	RR ← Input 10
$19	$8A	RR → Output 10
$1A	$1B	RR ← Input 11
$1B	$8B	RR → Output 11
$1C	$1C	RR ← Input 12
$1D	$8C	RR → Output 12
$1E	$1D	RR ← Input 13
$1F	$8D	RR → Output 13
$20	$1E	RR ← Input 14
$21	$8E	RR → Output 14
$22	$DD	Return program counter to $00, skip instruction at location $00. NOTE: The address is a "don't care;" $D is used for simplicity.

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extinguished when the system is in the battery back-up mode. The counter outputs also go to Figure 3, where they form the addressing for the 256×8 memory. The memory outputs ADDR-A, ADDR-B, ADDR-C, ADDR-D, INST-A, INST-B, INST-C, and INST-D then return to form the I/O selection and microprocessor instructions (Figure 2).

From Figure 2, real world inputs enter the system via connector J1 and mux U3; simulated inputs enter via mux U37 from switches. R53 and R54 are provided to limit current during an STO or STOC instruction when OEN is disabled, since the U37 mux and the U6 ICU will be accessing the data bus simultaneously. Similarly, R28 performs current limiting during these instructions. R13 through R27 perform the same function as R53 and R54 and in addition, protect U3 against electrostatic damage (reference **Motorola CMOS Data Book, Series C**, page 5-4, item number 12). Selector switch S3 controls whether the inputs come from the real world or the switches by gating the WRITE/$\overline{\text{READ}}$ signal to the inhibit inputs of U3 and U37.

Outputs exit the system via connector J2 and output display LEDs D8 through D23 indicate the logic levels of the 16 outputs.

From Figure 3, clock signal X1 enters U29, pin 11 and causes one shot U30 to generate a delayed pulse at pin 10. The delayed pulse is ORed with STROBE by U17 which results in a pulse ($\overline{\text{ST}}$) at U17, pin 11 when: (1) the hex keypad is activated, or (2) X1 goes high. $\overline{\text{ST}}$ strobes the address (A0 through A7) into the memories U21 through U28.

Again from Figure 3, MEM-LOAD-STB is inverted and delayed by U15 and directed to steering gates U19. Steering is controlled by ÷2 counter U29. Additionally, the decimal points of the instruction and address seven-segment displays may be used to indicate whether the instruction or address is to be entered next from the keyboard. Use of the decimal points is optional.

From Figure 2, when the system is in the HALT mode (as determined by the HALT/RUN switch S4), the single step push button S2 enables the user to single step through the program while executing instructions by generating a pulse at gate U17, pin 10. This pulse feeds the clock input of U6 (MC14500B) and overrides R29.

When external power is present, the battery is trickle charged through diode D1 and R55. In addition, steering diode D1 directs external power to the CMOS circuitry.

The power failure detector senses the external power supply voltage via voltage divider and dropping diode R10, R9, and D3 and feeds the voltage to U35, pin 14. When the external power (V_{PS}) is not present, NO-PWR, $\overline{\text{NO-POWER}}$, and $\overline{\text{NO-PWR}}$ are active (true) which places the system in the low-power mode. Steering diode D2 directs battery power to the CMOS circuitry; D1 becomes a blocking diode to prevent battery discharge through the external power supply. The transient suppression diode's (D26's) zener voltage depends on the power supply voltage to be used.

The reader should note that the MC14049UB does not use pin 16; instead, pin 1 is connected to V_{DD}. In addition, if the system is to be operated at less than 6 volts, the current-limiting resistors to the indicator LEDs may be eliminated along with resistors R1 through R8.

TEST PROGRAM

The following test program may be used to trouble-shoot the development system. The program forces the output display LEDs to indicate the status of the system inputs. For example, when the input switch IN-O is switched to V_{DD}, output LED OUT-O turns on. When IN-O is switched to

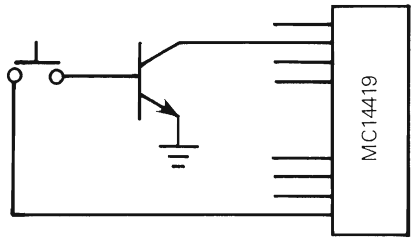

FIGURE 4. Use of Four External Transistors Allowing Operation with SPST Keyboard

TABLE 1. IC Power Connections

Designation	V_{DD}	V_{SS}
U1, U2	16	8
U3	24	12
U4 Through U12	16	8
U13 Through U20	14	7
U21 Through U28	24	12
U29	14	7
U30	16	8
U31	1	8
U32	14	7
U33, U34, U35	1	8
U36	14	7
U37	24	12

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